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PENNIE & EDMONDS
1155 AVENUE OF THE AMERICAS
NEW YORK, NY 100362711

EXAMINER
VIGUSHIN, JOHN B

ART UNIT	PAPER NUMBER
2827	

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49 (51)

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
08/082,328	Knight et al.
Examiner	**Art Unit**
John B. Vigushin	2841

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jun 26, 2001*.

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1, 28, 37-48, 52-59, 102, 143, 144, 146, 147, and 210-222* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1, 28, 37-47, 53-55, 58, 59, 102, 143, 144, 210-212, and 217-222* is/are rejected.

7) ☒ Claim(s) *48, 52, 56, 57, 146, 147, and 213-216* is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 47

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☒ Other: Response to Rule 312 Communication

DETAILED ACTION

Preliminaries

1. The information disclosure statement submitted on June 26, 2001 was filed after the mailing date of the Notice of Allowance on March 26, 2001 and simultaneously with the payment of the issue fee. The submission is in compliance with the provisions of 37 CFR 1.97(e) and 1.17(p). Accordingly, the petition is granted and the information disclosure statement is being considered by the examiner.

2. The amendment filed on June 26, 2001 under 37 CFR 1.312 has been entered.

3. Prosecution on the merits of this application is reopened on claims 1, 28, 37-48, 52-59, 102, 143, 144, 146, 147, and 210-222 considered unpatentable for the reasons indicated below:

4. Applicant is advised that the Notice of Allowance mailed March 26, 2001 is vacated. If the issue fee has already been paid, applicant may request a refund or request that the fee be credited to a deposit account. However, applicant may wait until the application is either found allowable or held abandoned. If allowed, upon receipt of a new Notice of Allowance, applicant may request that the previously submitted issue fee be applied. If abandoned, applicant may request refund or credit to a Deposit Account.

Claim Objections

5. Claims 53 and 220 are objected to because of the following informalities:

In Claim 53, line 1: delete "a".

In Claim 220, line 1: change "nodule" to --module--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 44, 46, 59 and 218 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Independent Claim 44 (see Amendment of February 25, 1998, Paper No. 24) recites the limitation "said chips" in line 6. There is insufficient antecedent basis for this limitation in the claim. This rejection may be overcome by changing "chips" to --chip-- in line 6.

Claim 46 recites a "greater dielectric **factor**" in line 2. What does **factor** mean? Is the Applicant referring to the dielectric *constant* (a high dielectric constant; a low dielectric constant)? The Examiner will interpret "dielectric factor" as **dielectric constant**.

Independent Claim 59 (see Examiner's Amendment in Notice of Allowance of March 26, 2001, Paper No. 45) recites the limitation "said chips" in line 5. There is insufficient antecedent basis for this limitation in the claim. This rejection may be overcome by changing "chips" to --chip-- in line 5.

Claim 218 recites "transverse to said conductive connection" in line 3. The entire limitation adds an indefinite transverse structure to the claim. Also, there is insufficient antecedent basis for "said conductive connection" in the claim.

Rejections Based On Prior Art

8. The following references were relied upon for the rejections hereinbelow:

Jacobsen (US 5,673,131) *Ballmer et al. (US 4,876,535)

Jacobsen (US 5,269,882) *Zappe (US 3,983,546)

*Already made of record in Applicant's Information Disclosure Statement filed on June 26, 2001 as Paper No. 47.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

10. Claims 1, 28, 37-39, 41, 53, 58, 102, 210-212, 217, 218 and 220 are rejected under 35 U.S.C. 102(b) as being anticipated by Zappe.

a) As to independent Claim 1, Zappe discloses, in Fig. 14, a substrate 116B; a chip 116A; means for powering chip 116A is the current supply for the Josephson tunneling parametrons which constitute the circuitry 162A and 164A of chip 116A; circuitry 162A and 164A are similar to the circuitry of 118A which comprise Josephson tunneling devices 118A (col.5: 4-12; col.9: 56-58; col.10: 4-6; col.12: 40-48); means 170A, 172A (on chip 116A) and 170B, 172B (on substrate 116B) for capacitively signalling between chip 116A and substrate 116B (col.12: 58-67).

a1) As to Claim 37, Zappe further discloses, in Fig. 14, first and second coupled half-capacitors (first half-capacitor 170A, associated with chip 116A, is coupled to second half-capacitor 170B, associated with substrate 116B; first half-capacitor 172A, associated with chip 116A, is coupled to second half-capacitor 172B, associated with substrate 116B; col.12: 58-62), the first and second half-capacitors comprising effectively overlapping conductive regions separated by a gap (Fig. 14 and col.12: 62-67).

a2) As to Claim 38, Zappe further discloses that at least one of the conductive regions comprises a plate (col.12: 58-62).

a3) As to Claim 39, the capacitance of means 170A, 170B, 172A, 172B of Zappe *inherently* can be varied by changing the effective area of overlap between the conductive regions.

a4) As to Claim 41, Zappe further discloses that the gap is at least partially filled with a dielectric (i.e., at least part of the material of chip 116A that separates first half capacitors 170A, 172A from second half-capacitors 170B and 172B; Fig. 14).

a5) As to Claim 53, Zappe further discloses a plurality of coupled half-capacitors (i.e., half-capacitor 170A is coupled with half-capacitor 170B; half-capacitor 172A is coupled with half-capacitor 172B; see Fig. 14 and col.12: 58-67); a substantial area of chip 116A and a substantial portion of the area of substrate 116B being covered with effectively overlapping half-capacitors (170A and 172A effectively overlapping 170B and 172B, respectively; see Fig. 14).

a6) As to Claim 58, Zappe further discloses, in Fig. 14, that first half-capacitor 170A (associated with chip 116A) overlays circuitry (i.e., the circuitry of substrate 116B).

a7) As to Claim 210, Zappe further discloses a transmission line 166 coupled to a first means 170A for capacitively signalling (Fig. 14; col.12: 46-48).

a8) As to Claim 211, Zappe further discloses that transmission line 166 is further coupled (through half-capacitor 170A) to a second means 170B for capacitive signalling (Fig. 14; col.12: 58-60).

a9) As to Claim 212, Zappe further discloses that transmission line 166 is further coupled to a conductive junction 162A (Fig. 14; col.12: 40-48).

b) As to independent Claim 28, Zappe discloses, in Fig. 14, a chip 116A; a substrate 116B; a plurality of electronic devices 162A, 164A implemented on chip 116A (col.12: 40-48); a signal lead 166 of at least one of the plurality of electronic devices 162A, 164A (i.e., device 162A) coupled to a first half-capacitor 170A attached to chip 116A (col.12: 46-48); a second half-capacitor 170B attached to substrate 116B (col.12: 49-50) coupling a signal to first half-capacitor 170A (col.12: 58-67).

c) As to independent Claim 102, Zappe discloses, in Fig. 14, a first module 116A having a plurality of electronic devices in circuitry 162A (col.12: 40-48; the electronic devices of circuitry 162A are similar to the electronic devices OSC.1-OSC.N in 118A shown in Figs. 13A,B as indicated in col.12: 40-46); a first half-capacitor 170A and at least one signal lead 166 connecting electronic devices of circuitry 162A to first half-capacitor 170A; a second module 116B having a second half-capacitor 170B; first and second modules 116A and 116B being positioned such that first and second half-capacitors 170A and 170B provide a capacitive signal path between first and second modules 116A and 116B (col.12: 58-67).

c1) As to Claim 217, Zappe further discloses, in Fig. 14, further paired half-capacitors 172A and 172B such that the capacitive signal path is distributed among multiple capacitors (i.e., capacitors 170A/170B and 172A/172B; col.12: 58-67).

c2) As to Claim 218, Zappe further discloses, in Fig. 14, that first module 116A is positioned relative to second module 116B (i.e., positioned above second module 116B). The limitation "by motion transverse to said capacitive signal path transverse to said conductive connection" is a process limitation in a product claim and cannot serve to patentably define the product over the prior art of record, in this case Zappe. See Product-by-Process in MPEP § 2113 and 2173.05(p).

c3) As to Claim 220, Zappe further discloses, in Fig. 14, that first module 116A includes a transmission line 166 that is connected to a plurality of transmission lines which interconnect the

electronic components in circuitry 162A (see Fig. 13A, the transmission lines connecting the PUMP components in circuitry 118A, similar to circuitry 162A; col.12: 40-46).

11. Claims 102, 143, 144, 217, 218, 221 and 222 are rejected under 35 U.S.C. 102(b) as being anticipated by Ballmer et al.

a) As to independent Claim 102, Ballmer et al. discloses, in Fig. 2, a first module 20 (data carrier) having a plurality of electronic devices 23a-23n (Fig. 2), a first half-capacitor 22a and at least one signal lead connecting the electronic devices 23a-23n to first half-capacitor 22a (Fig. 2); a second module 25 (data reader) having a second half-capacitor 27a, the modules 20 and 25 being positioned such that the first and second half-capacitors 22a and 27a provide a capacitive signal path between the first and second modules 20 and 25 (Abstract; col.2: 48-50; col.3: 14-17 and 31-47).

a1) As to Claim 143, Ballmer et al. further discloses that first and second half-capacitors 22a and 27a of Fig. 2 (analogous to half-capacitors 11 and 16 in Fig. 1) are shaped such that the admittance of the capacitive signal path is substantially unaffected by a small misalignment between the first and second modules 20 and 25 (i.e., col.3: 14-17: "the capacitance C of the capacitor C1 fluctuates only within prescribable limits" implies that the admittance of the capacitive signal path is substantially unaffected by a small misalignment between the first and second modules 10 (20) and 15 (25) inherently due to the mechanical guidance means of the first module 10(25)).

a2) As to Claim 144, Balmer et al. further discloses that area of one of the half-capacitors (common electrode 21) is greater than the area of the other of the half-capacitors, i.e., half-capacitor 16 (Fig. 3).

a3) As to Claim 217, Ballmer et al. further discloses, in Fig. 2, further paired half-capacitors 29a-n and 22a-n such that the capacitive signal path is distributed among multiple capacitors C1-Cn.

a4) As to Claim 218, Ballmer et al. further discloses, in an embodiment combining the embodiments of Figs. 2 and 3, the first module 30 is positioned relative to the second module 35 by motion transverse to the capacitive signal path (col.4: 1-12).

a5) As to Claims 221 and 222, Ballmer et al. further discloses means for varying the admittance of the capacitive signal path by changing the effective area of overlap between the half-capacitors (Figs. 2 and 3), wherein the means for varying the admittance includes mechanical devices (motor M; col.3: 53-58).

12. Claims 1, 28, 37-39, 41, 42, 58, 102, 210-212 and 217-220 are rejected under 35 U.S.C. 102(e) as being anticipated by Jacobsen.

Examiner's Note: Claims 1 and 28 use two references to reject under 35 USC 102(e) in accordance with MPEP § 2131.01. The two references are US 5,673,131 (hereinafter referred to as Jacobsen '131) and US 5,269,882 (hereinafter referred to as Jacobsen '882), the latter being incorporated by reference into the former (see Jacobsen '131: col.1: 45-48 and col.4: 5-6).

a) As to Claim 1, Jacobsen '131 discloses, in Fig. 9b: a substrate 212; a chip 210 [*Examiner's Note*: Substrate 210 is a non-conductive inorganic material (Jacobsen '882: col.4: 24-25) that is coated with various material layers including a P or N type semiconductor material and electron beam resist (Jacobsen '882: col.4: 27-31 and 43-46); electron beam lithography processes are performed and, thereafter, electronic components are formed by doping the semiconductor material, and circuit patterns are formed by sputtering, chemical vapor deposition, etc. followed by electron beam lithography processes (Jacobsen '882: col.4: 64-67; col.5: 3-41). *Because substrate 210 includes a doped and metallized semiconductor material comprising electronic devices and interconnection circuitry, the Examiner takes the position that substrate 210 is a cylindrically shaped chip*]; means for powering chip 210 (Jacobsen '131: col.4: 3-6 in conjunction with col.1: 45-48; col.4: 14-16); means (half-capacitor plates 216 and 214 for capacitively signalling between chip 210 and substrate 212 (Jacobsen '131: col.7: 13-22); signal leads connected on substrate 212 and chip 210 to means 216 and 214 for capacitively signalling (Jacobsen '131: Fig. 9b; col.6: 60-64).

a1) As to Claim 37, Jacobsen '131 further discloses, in Fig. 9b, first and second coupled half-capacitors (first half-capacitor 216, associated with chip 210, is coupled to second half-capacitor 214, associated with substrate 212), the first and second half-capacitors 216 and 214 comprising effectively overlapping conductive regions separated by a gap.

a2) As to Claim 38, Jacobsen '131 further discloses that at least one of the conductive regions comprises a plate (col.7: 13-16).

a3) As to Claim 39, the capacitance of means 216 and 214 of Jacobsen '131 *inherently* can be varied by changing the effective area of overlap between the conductive regions (plates 216 and 214).

a4) As to Claim 41, Jacobsen '131 further discloses that the gap is at least partially filled with a dielectric (Fig. 9b).

a5) As to Claim 42, the dielectric of Jacobsen '131 (Fig. 9b; col.7: 24-32) is *inherently* uniform because, if it were not, there would be random errors generated in the electric field strength between the half-capacitors 216 and 214, i.e., noise due to unpredictable fluctuations in the dielectric constant.

a6) As to Claim 58, Jacobsen '131 further discloses, in Fig. 9b, that first half-capacitor 216 (associated with chip 210) overlays circuitry (i.e., the circuitry of substrate 212).

a7) As to Claim 210, Jacobsen '131 further discloses, in Fig. 9b, a transmission line coupled to a first means 216 for capacitively signalling (the transmission line is shown connecting circuit 218 and half-capacitor 216).

a8) As to Claim 211, Jacobsen '131 further discloses, in Fig. 9b, that the transmission line is further coupled capacitively to a second means 214 for capacitively signalling.

a9) As to Claim 212, Jacobsen'131 further discloses, in Fig. 9b, that the transmission line is further coupled to a conductive junction 218.

b) As to independent Claim 28, Jacobsen '131 discloses, in Fig. 9b: a chip 210 [*Examiner's Note*: Substrate 210 is a non-conductive inorganic material (Jacobsen '882: col.4:

24-25) that is coated with various material layers including a P or N type semiconductor material and electron beam resist (Jacobsen '882: col.4: 27-31 and 43-46); electron beam lithography processes are performed and, thereafter, electronic components are formed by doping the semiconductor material, and circuit patterns are formed by sputtering, chemical vapor deposition, etc. followed by electron beam lithography processes (Jacobsen '882: col.4: 64-67; col.5: 3-41). *Because substrate 210 includes a doped and metallized semiconductor material comprising electronic devices and interconnection circuitry, the Examiner takes the position that substrate 210 is a cylindrically shaped chip*]; a substrate 212; a plurality of electronic devices 218 implemented on chip 210 (Jacobsen '131: col.4: 3-6 and 10-14; col.7: 20-21); a signal lead of at least one of the plurality of electronic devices 218 coupled to a first half-capacitor 216 attached to chip 210 (Jacobsen '131: Fig. 9b; col.6: 60-64; col.7: 16-21: the signal lead between half-capacitor 216 and at least one of electronic devices 218, as shown in Fig. 9b, is how the capacitively transmitted information is "passed from first half-capacitor 216 to circuit component 218" in col.7: 20-21); a second half-capacitor 214 attached to substrate 212 and capacitively coupling a signal to first half-capacitor 216 (Jacobsen '131: col.7: 13-22).

c) As to independent Claim 102, Jacobsen '131 discloses, in Fig. 9b, a first module 210 having a plurality of electronic devices 218 (col.4: 3-6 and 10-14; col.7: 20-21); a first half-capacitor 216 and at least one signal lead connecting electronic devices 218 to first half-capacitor 216 (Fig. 9b; col.6: 60-64; col.7: 16-21: the signal lead between half-capacitor 216 and at least one of electronic devices 218, as shown in Fig. 9b, is how the capacitively transmitted information

is "passed from first half-capacitor 216 to circuit component 218" in col.7: 20-21); a second module 212 having a second half-capacitor 214, the modules 210 and 212 being positioned such that the first and second half-capacitors 216 and 214 provide a capacitive signal path between first and second modules 210 and 212 (col.7: 13-22).

c1) As to Claim 217, Jacobsen '131 discloses, in Fig. 9b, further paired half-capacitors (right end of Fig. 9b where the arrow is between the half-capacitors) such that the capacitive signal path is distributed among multiple capacitors (i.e., the capacitor formed by half-capacitors 216 and 214 on the left end and the above-mentioned paired half-capacitors on the right end of Fig. 9b).

c2) As to Claim 218, Jacobsen '131 discloses, in Fig. 9b, that first module 210 is positioned relative to second module 212 (i.e., adjacent and parallel). The limitation "by motion transverse to said capacitive signal path transverse to said conductive connection" is a process limitation in a product claim and cannot serve to patentably define the product over the prior art of record, in this case, Jacobsen '131. See Product-by-Process in MPEP § 2113 and 2173.05(p)].

c3) As to Claim 219, Jacobsen '131 discloses that second module 212 is a cable (Figs. 1 and 9b) including at least one non-coaxial wire (i.e., the wires on the module surface; Fig. 9b).

c4) As to Claim 220, Jacobsen '131 discloses that first module 210 further includes a transmission line (e.g., between half-capacitor 216 and circuit 218) that is connected to a plurality of transmission lines on the surface of module 210 (Fig. 9b).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 40, 43, 45, 47, 54 and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zappe.

a) As to Claim 40:

I. Zappe discloses all the limitations of Claim 39 including a chip 116A with wiring 166, 168 and electronic devices 162A, 164A fabricated thereon but does not teach that portions of the chip 116A are passivated, said portions not including the first half-capacitor 170A or 172A.

II. Passivating layers either deposited or epitaxially grown on a circuitized chip surface are old and well-known in the art to protect the chip circuitry from contamination and interconnection shorts.

III. Since Zappe teaches joining chip 116A and substrate 116B (Fig. 14) for the purpose of capacitively coupling half-capacitors 170A/170B and 172A/172B, it would have been obvious to one of ordinary skill in the art at the time the invention was made to passivate at least the chip portions carrying the circuitry 162A, 164A and wiring 166, 168 of chip 116A in order to protect said circuitry and wiring from, at the very least, environmental contamination and,

furthermore, not to passivate the half-capacitors 170A and 172A in order to expose them to external reading devices that can access the capacitively generated signals from half-capacitors (plates) 170A and 172A.

b) As to Claim 43:

I. Zappe discloses the limitations of Claim 42 but does not indicate that the chip material 116A is uniform.

II. However, it is well-known to use a uniform chip substrate material in order to provide a substrate with uniform electrical and mechanical attributes for effective fabrication of the electronic devices and wiring thereon and proper functioning of the resultant chip circuitry.

III. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a uniform material in order to better control the electrical characteristics, such as dielectric constant, for the proper function of the Josephson tunneling device circuitry and capacitive signalling taught by Zappe, and for ensuring the effective fabrication of the Josephson electronic devices 162A, 164A and wiring 166, 168 thereon.

c) As to Claim 45:

I. Zappe discloses the limitations of Claim 41 but does not teach a passivation distinct from the dielectric material from chip 116A.

II. Passivating layers either deposited or epitaxially grown on a circuitized chip surface (i.e., distinct from the dielectric material of the chip) are old and well-known in the art to protect the chip circuitry from contamination and interconnection shorts.

III. Since Zappe teaches joining chip 116A and substrate 116B (Fig. 14) for the purpose of capacitively coupling half-capacitors 170A/170B and 172A/172B, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a deposited or epitaxially grown passivation layer on at least the chip portions carrying the circuitry 162A, 164A and wiring 166, 168 of chip 116A in order to protect said circuitry and wiring from, at the very least, environmental contamination.

d) As to Claim 47:

I. Zappe further discloses that the dielectric material of chip 116A is joined to substrate 116B (Fig. 14) but does not indicate how chip 116A is affixed to 116B.

II. Bonding materials such as solder, conductive and non-conductive adhesives, and B-staged dielectric materials are old and well-known in the art as materials for affixing chips to substrates.

III. Since Zappe teaches that chip 116A and substrate 116B are joined (Fig. 14) it would have been obvious to one of ordinary skill in the art at the time the invention was made to bond chip 116A to substrate 116B in order establish a secure mechanical connection of 116A to 116B and thereby ensure reliable capacitive signalling between chip 116A and substrate 116B.

e) As to Claim 54:

I. Zappe discloses all the limitations of Claim 53 but does not teach that at least one half-capacitor 170A, 172A on chip 116A is connected to a chip ground, power, or other common reference signal.

II. It is old and well-known in the art for a plate of a coupling capacitor to be connected to a reference point (ground, power or a common reference signal, e.g., a chip-specific datum point) in order to charge/discharge in accordance with an ac signal to be passed to or received from another stage of circuitry on the chip, or another stage of circuitry on an external substrate to which the chip is mounted, wherein the dc component is blocked in order for the signal to be usable in the next stage of circuitry.

III. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to connect at least one half-capacitor 170A or 172A to a chip ground, power, other common reference signal in order to pass and properly match the ac signals out of circuitry 162A, 164A (OSC.1-OSC.N; see Fig. 13B; col.12: 40-48) of chip 116A to the next stage of circuitry 162B, 164B (J1-JN; see Fig. 13B; col.12: 49-57) in substrate 116B.

f) As to Claim 55:

I. Zappe discloses all the limitations of Claim 53 but does not teach that at least one half-capacitor 170B, 172B on substrate 116B is connected to a substrate ground, power, or other common reference signal.

II. It is old and well-known in the art for a plate of a coupling capacitor to be connected to a reference point (ground, power or a common reference signal, e.g., a substrate-specific datum point) in order to charge/discharge in accordance with an ac signal to be passed to or received from another stage of circuitry on the substrate, or another stage of circuitry on an

external chip mounted to the substrate, wherein the dc component is blocked in order for the signal to be usable in the next stage of circuitry.

III. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to connect at least one half-capacitor 170B or 172B to a substrate ground, power, other common reference signal in order to receive and properly match the ac signals out of circuitry 162A, 164A (OSC.1-OSC.N; see Fig. 13B; col.12: 40-48) of chip 116A to the next stage of circuitry 162B, 164B (J1-JN; see Fig. 13B; col.12: 49-57) in substrate 116B.

15. Claims 40 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobsen '131.

a) As to Claim 40:

I. Jacobsen '131 discloses all the limitations of Claim 39 including a chip 210 with wiring and electronic devices 218 fabricated thereon but does not teach that portions of the chip 210 are passivated, said portions not including the first half-capacitor 216.

II. Passivating layers either deposited or epitaxially grown on a circuitized chip surface are old and well-known in the art to protect the chip circuitry from contamination and interconnection shorts, where, at the very least, protection from environmental contamination would have been recognized as beneficial in the pertinent art of Jacobsen '131.

III. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to passivate at least the wiring and electronic device portions 218 of chip 210 with a layer of deposited or epitaxially grown insulation in order to protect said wiring

and electronic devices from, at the very least, environmental contamination and, furthermore, not to passivate first half-capacitor 216 in order to expose first half-capacitor 216 for the purpose of performing the disclosed capacitive signalling between chip 210 and substrate 212.

b) As to Claim 45:

I. Jacobsen '131 discloses all the limitations of Claim 41 including a chip 210 with wiring and electronic devices 218 fabricated thereon but does not teach including a passivation distinct from the dielectric.

II. Passivating layers either deposited or epitaxially grown on a circuitized chip surface are old and well-known in the art to protect the chip circuitry from contamination and interconnection shorts, where, at the very least, protection from environmental contamination would have been recognized as beneficial in the pertinent art of Jacobsen '131.

III. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to passivate at least the wiring and electronic device portions 218 of chip 210 with a layer of deposited or epitaxially grown insulation, distinct from the dielectric, in order to protect said wiring and electronic devices from, at the very least, environmental contamination.

16. Claims 53-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobsen '131 in view of Zappe.

a) As to Claim 53:

I. Jacobsen '131 discloses all the limitations of Claim 37 including a half-capacitor 216 on chip 210 overlapping a half-capacitor 214 on substrate 212 for capacitive signalling of the output signals of circuit components 218 on chip 210 to the circuit components on substrate 212 but does not teach a plurality of coupled half-capacitors, a substantial area of chip 210 and a substantial portion of the area of substrate 212 being covered with effectively overlapping half-capacitors.

II. Zappe discloses, in Fig. 4, a circuit with a plurality (162A and 164A) of electronic circuit components on chip 116A respectively connected by output traces to a *plurality* (170A and 172A) of half-capacitors which, by capacitive signalling, wirelessly send the signals to a corresponding plurality (162B and 164B) of electronic circuit components on substrate 116B by way of half-capacitors 170B and 172B.

III. Since Jacobsen '131 and Zappe are both in the art of electronic devices utilizing capacitive signalling, the use of plural half-capacitors associated with plural electronic circuit devices on a chip for capacitively communicating with plural electronic circuit devices on another adjacent substrate, as taught by Zappe, would have been readily recognized in the pertinent art of Jacobsen '131.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the chip 210 and substrate 212 of Jacobsen '131 to each include a *plurality* of electronic circuit components 218, as taught in Fig. 14 of Zappe, respectively wired to a plurality of half-capacitors that capacitively pass signals from chip 210

to/from substrate 212 in order to enable any number of circuit elements as required on chip 210 to wirelessly communicate with corresponding circuit elements on substrate 212 by capacitive signalling.

b) As to Claim 54:

I. Modified Jacobsen '131 discloses all the limitations of Claim 53 but does not teach that at least one half-capacitor 216 on chip 210 is connected to a chip ground, power, or other common reference signal.

II. It is old and well-known in the art for a plate of a coupling capacitor to be connected to a reference point (ground, power or a common reference signal, e.g., a chip-specific datum point) in order to charge/discharge in accordance with an ac signal to be passed to or received from another stage of circuitry on the chip, or another stage of circuitry on an external substrate to which the chip is mounted, wherein the dc component is blocked in order for the signal to be usable in the next stage of circuitry.

III. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to connect at least one half-capacitor 216 of modified Jacobsen '131 to a chip ground, power, other common reference signal in order to perform capacitive signalling between the ac signals of electronic circuitry 218 of chip 210 and an adjacent stage of circuitry corresponding to electronic circuit 218 in substrate 212.

c) As to Claim 55:

I. Modified Jacobsen '131 discloses all the limitations of Claim 53 but does not teach that at least one half-capacitor 214 on substrate 212 is connected to a substrate ground, power, or other common reference signal.

II. It is old and well-known in the art for a plate of a coupling capacitor to be connected to a reference point (ground, power or a common reference signal, e.g., a substrate-specific datum point) in order to charge/discharge in accordance with an ac signal to be passed to or received from another stage of circuitry on the substrate, or another stage of circuitry on an external chip mounted to the substrate, wherein the dc component is blocked in order for the signal to be usable in the next stage of circuitry.

III. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to connect at least one half-capacitor 214 of modified Jacobsen '131 to a substrate ground, power, other common reference signal in order to perform capacitive signalling between the ac signals of electronic circuitry on substrate 212 and an adjacent stage of electronic circuitry 218 in chip 210.

Allowable Subject Matter

17. Claims 44 and 59 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

18. Claim 46 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

19. Claims 48, 52, 56, 57 and 213-216 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

20. The following is a statement of reasons for the indication of allowable subject matter:

As to independent Claim 44, patentability resides in *a power connector extending through the dielectric*, in combination with the other limitations of the claim.

As to Claim 46, patentability resides in that *the dielectric has a greater "dielectric factor" (i.e., dielectric constant) than the passivation*, in combination with the other limitations of the claim.

As to Claim 48, patentability resides in that *the dielectric provides a means for affixing the chip to the substrate*, in combination with the other limitations of the claim.

As to Claim 52, patentability resides in that *the means for capacitively signalling operates despite a substantial misalignment between the substrate and the chip*, in combination with the other limitations of the claim.

As to Claim 57, patentability resides in that *the shape of one of the conductive regions differs from the shape of the other of the conductive regions*, in combination with the other limitations of the claim.

As to independent Claim 59, patentability resides in *an additional half-capacitor associated with one of the chip and the substrate*, in combination with the other limitations of the claim.

As to Claims 213 and 215, patentability resides, at least in part, in that *the second area is larger than the first area*, in combination with the other limitations of Claims 213 and 215, respectively.

As to Claims 214 and 216, patentability resides, at least in part, in that *the second pitch is larger than the first pitch*, in combination with the other limitations of Claims 214 and 216, respectively.

21. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Vigushin whose telephone number is (703) 308-1205. The examiner can normally be reached on Monday to Friday from 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Talbott, can be reached on (703) 305-9883. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7382.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

John B. Vigushin
Patent Examiner
January 10, 2002

Jayprakash N. Gandhi
Primary Examiner
Technology Center

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Response to Rule 312 Communication

☐ The petition filed _____ under 37 CFR 1.312(b) is granted. The paper has been forwarded to the examiner for consideration on the merits.

_____
_____
Director,
Patent Examining Group _____

☑ The amendment filed June 26, 2001 under 37 CFR 1.312 has been considered, and has been:

☑ entered.

☐ entered as directed to matters of form not affecting the scope of the invention (Order 3311).

☐ disapproved. See explanation below.

☐ entered in part. See explanation below.

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* U.S. GPO: 1996-404-